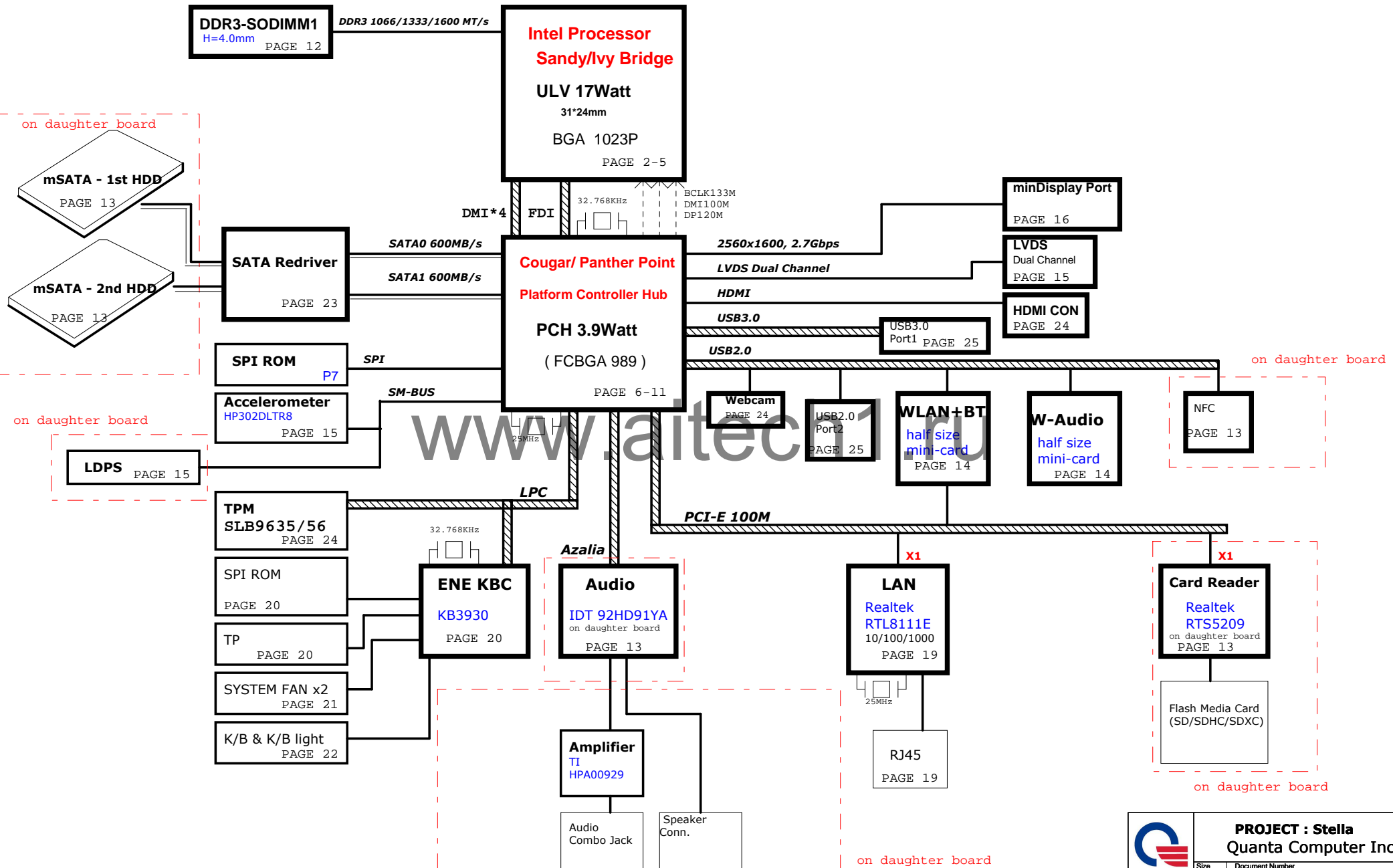
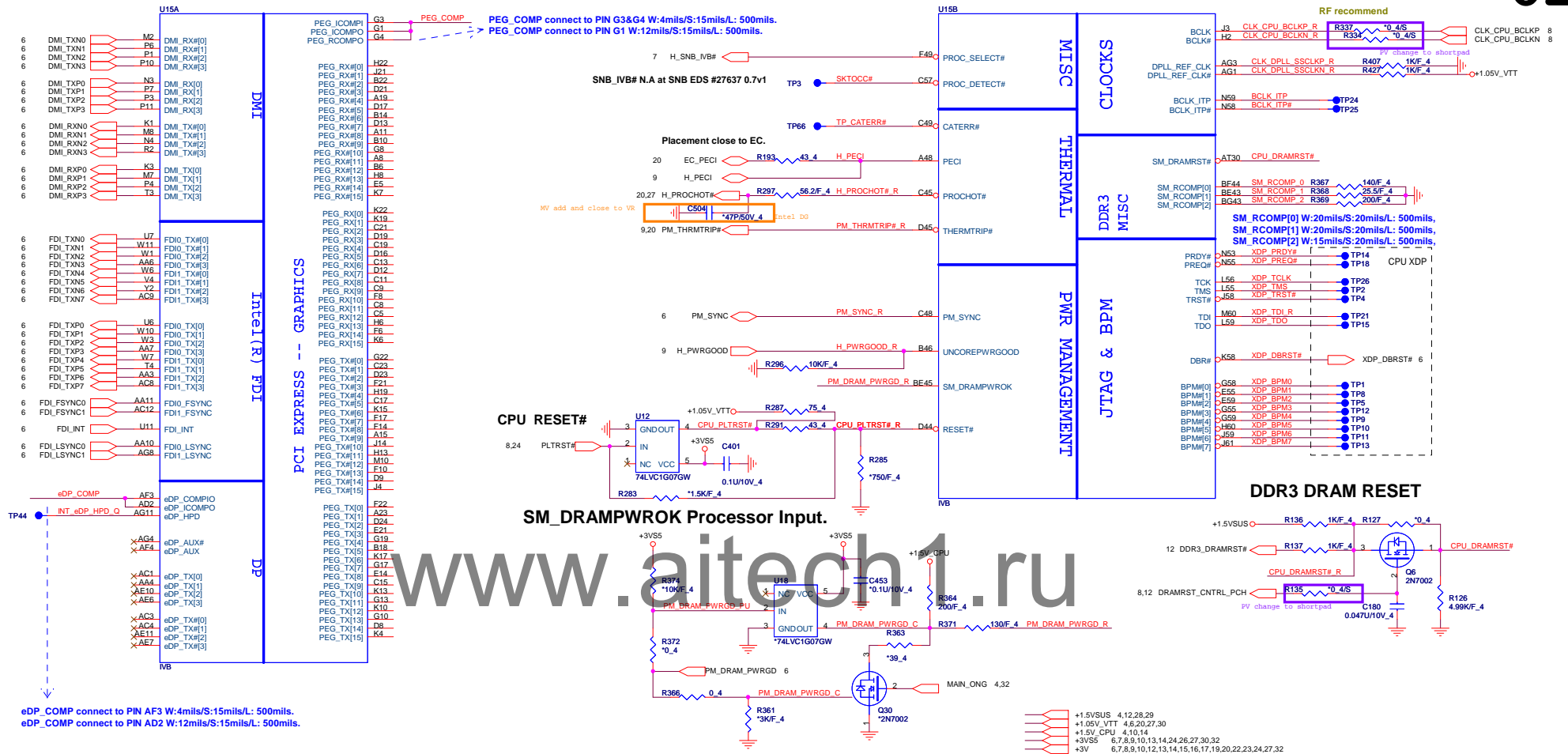


14" Envy Huron/Chief River ULV 17W(BGA) UMA BLOCK DIAGRAM

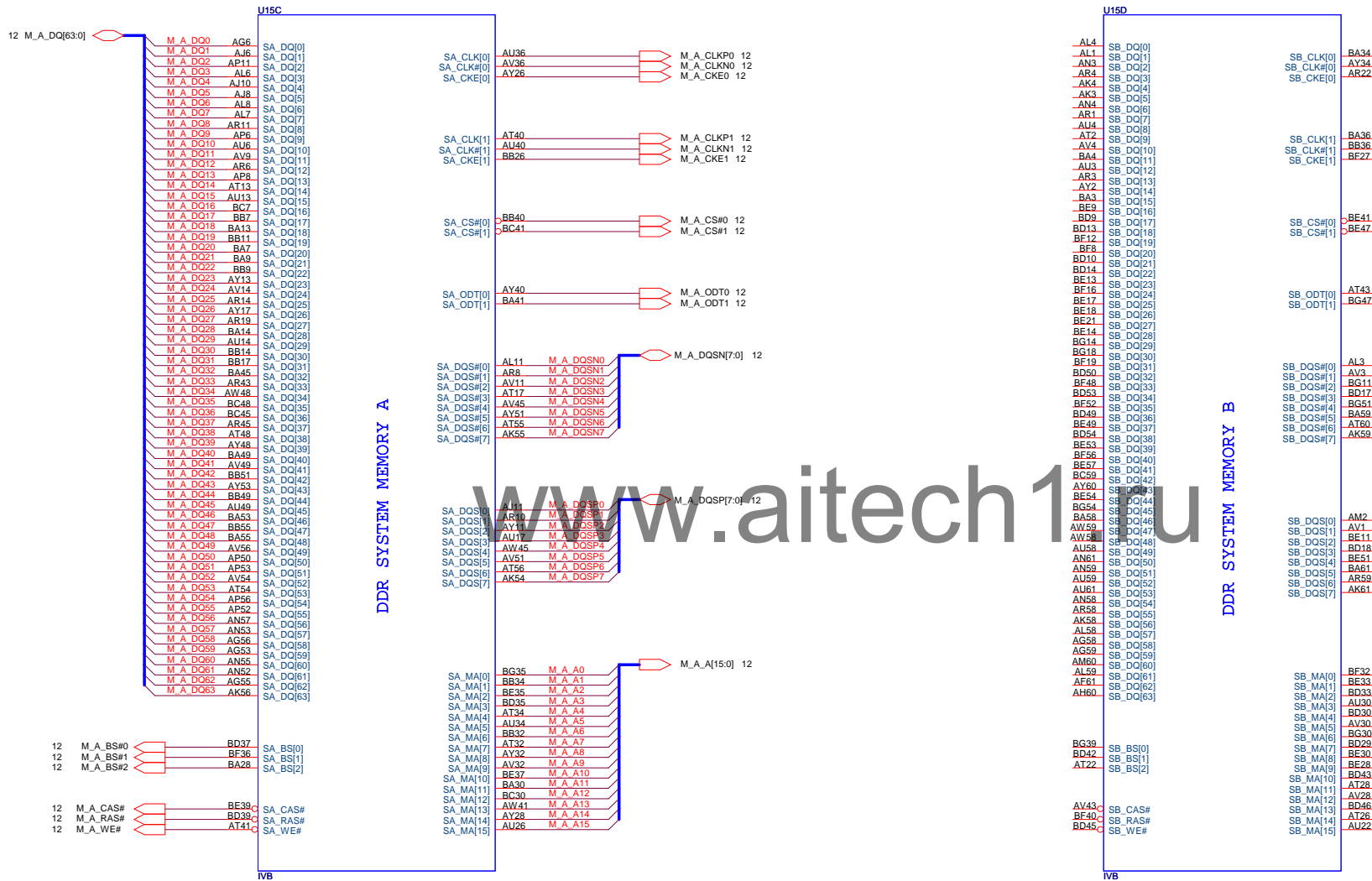
01



04232012_factory_me



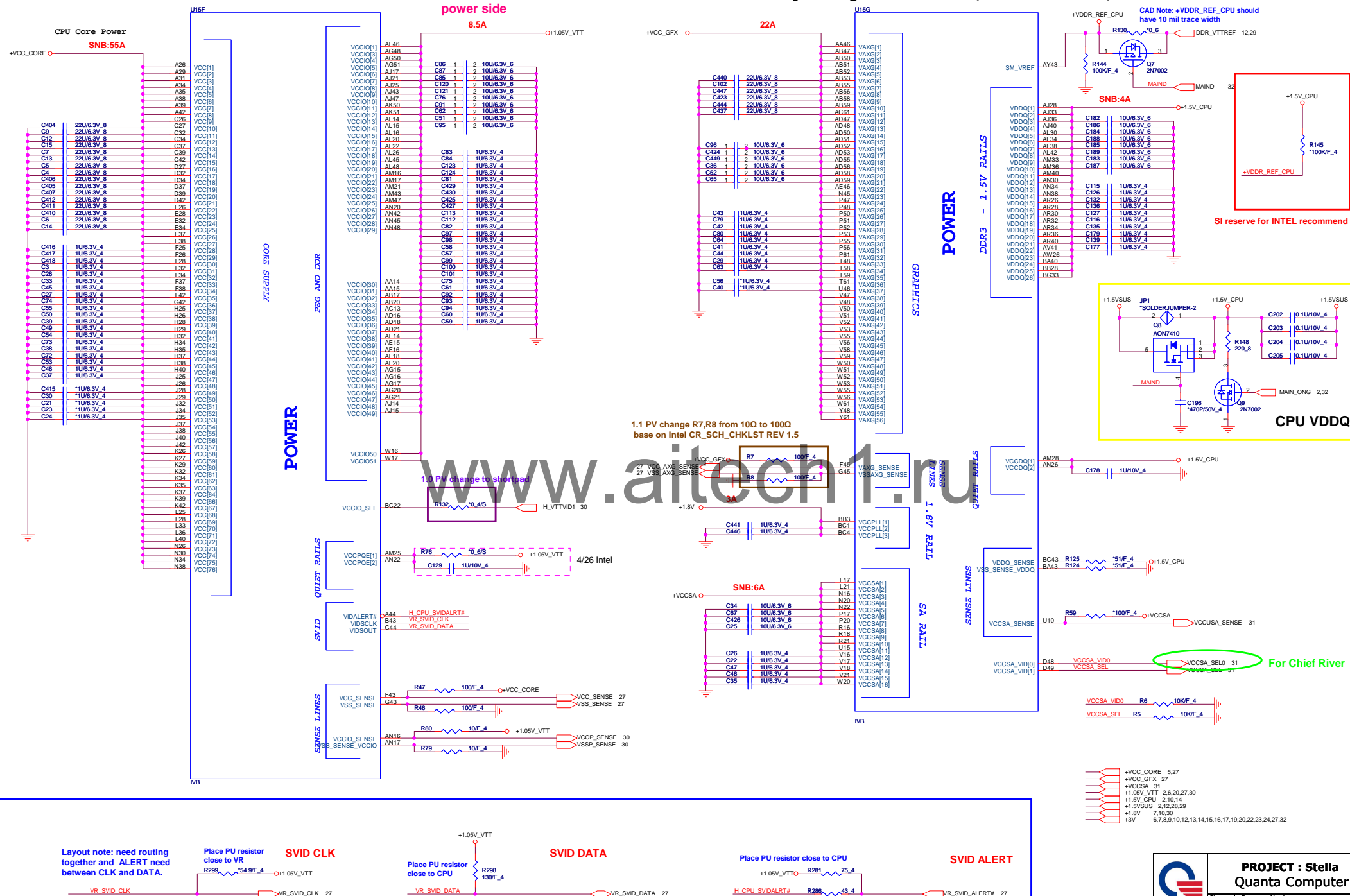
Ivy Bridge Processor (DDR3)



Ivy Bridge Processor (POWER)

Ivy Bridge Processor (GRAPHIC POWER)

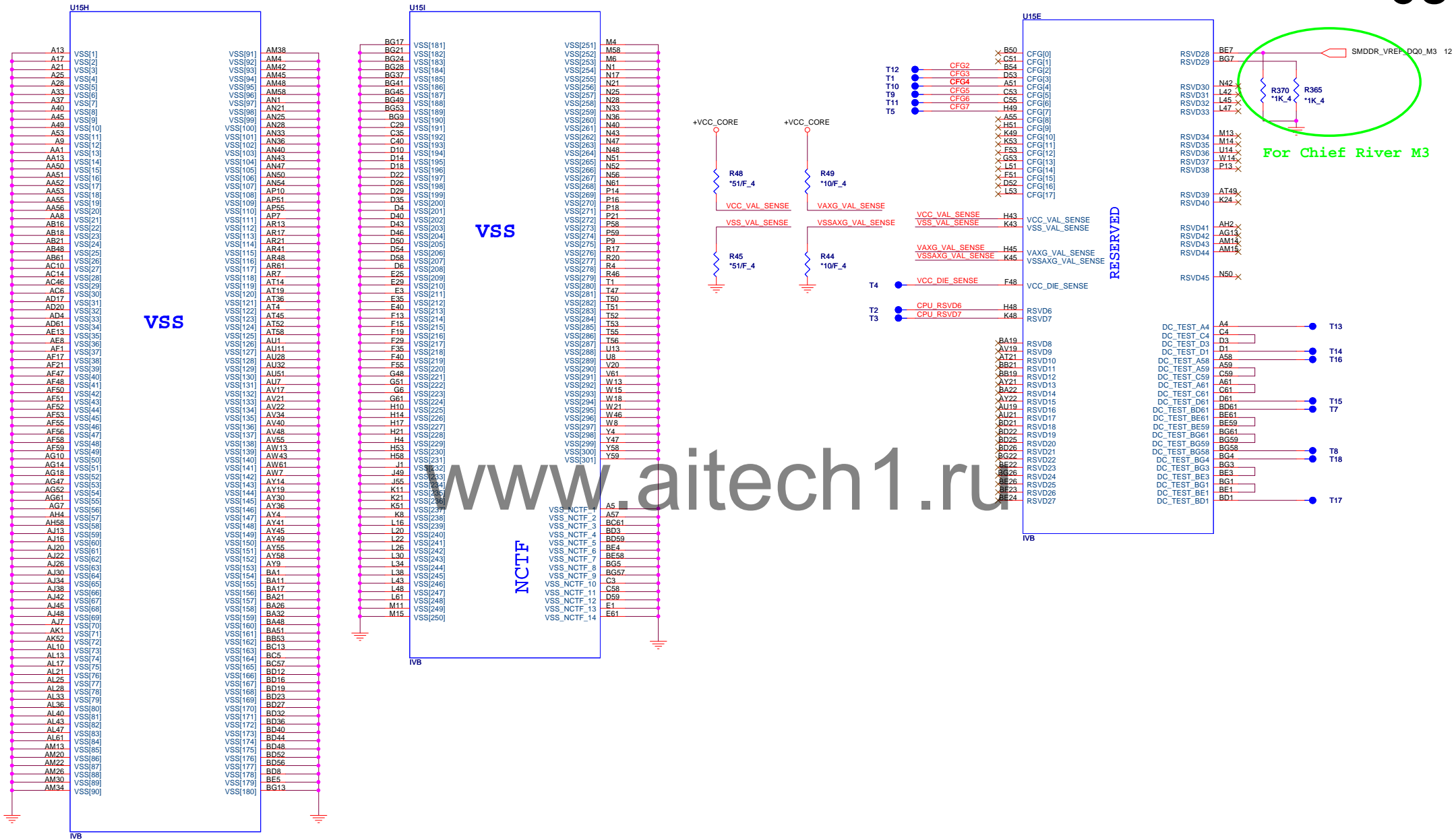
Ivy Bridge Processor (GRAPHIC POWER)



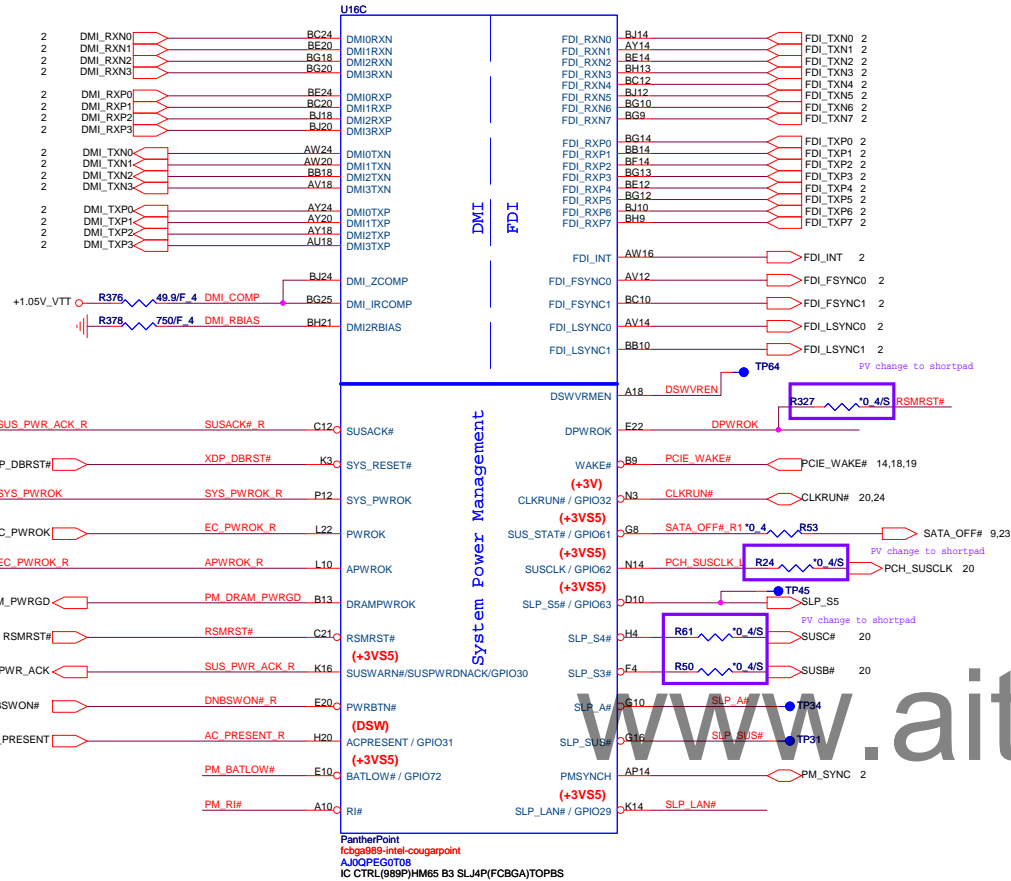
Ivy Bridge Processor (GND)

Ivy Bridge Processor (RESERVED, CFG)

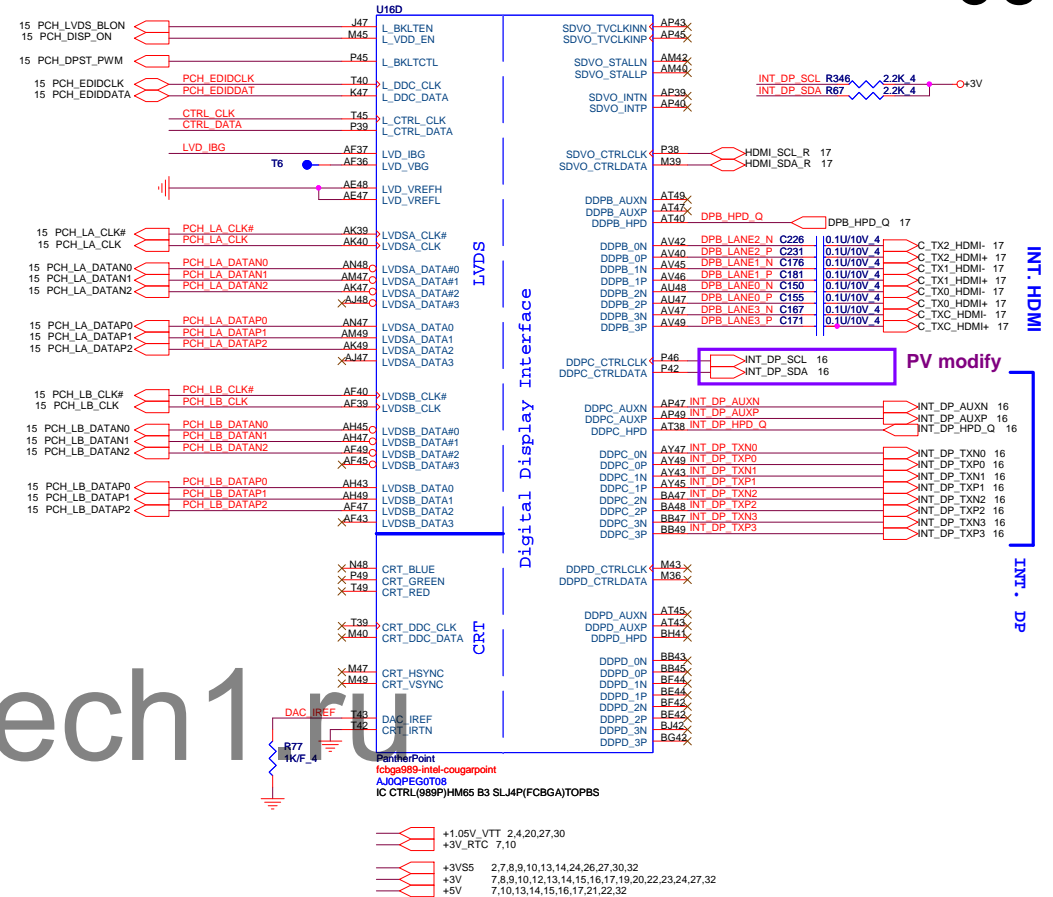
05



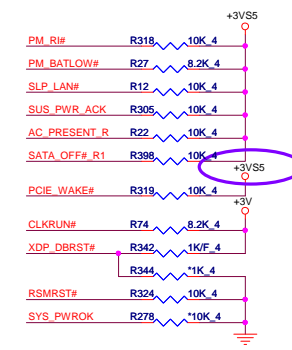
Panther Point (DMI,FDI,PM)



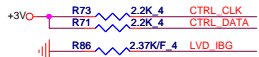
Panther Point (LVDS,DDI)



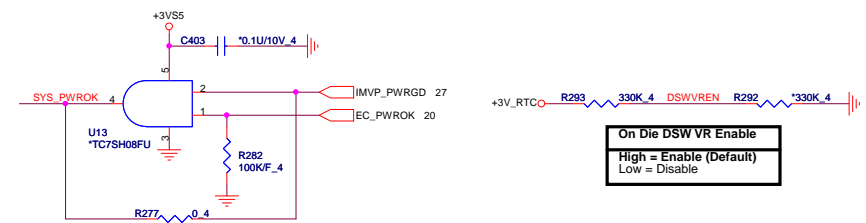
PCH Pull-high/low(CLG)



**INT LVDS & CRT disable
(DIS only remove)**

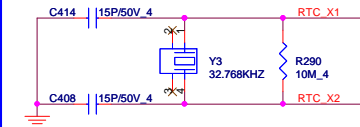


System PWR_OK(CLG)

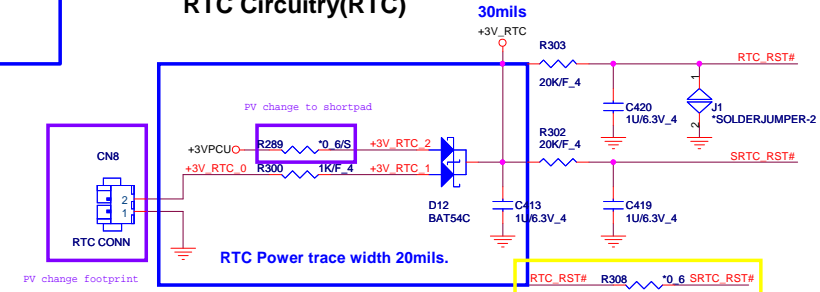


PROJECT : Stella
Quanta Computer Inc.

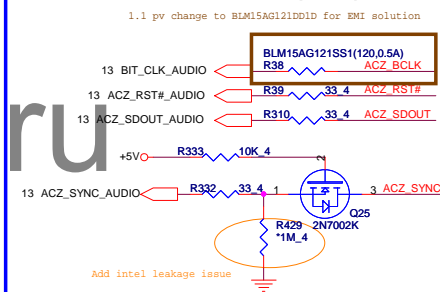
Size Custom	Document Number PCH 1/6 (DMI/FDI/VIDEO)	Rev 1A
Date: Monday, April 23, 2012		Sheet 6 of 31



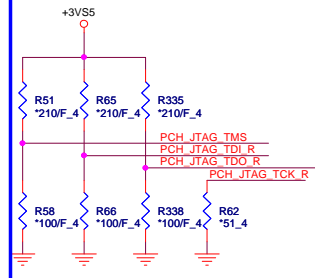
RTC Circuitry(RTC)



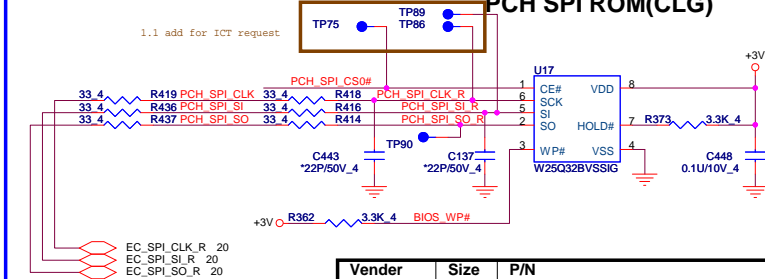
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

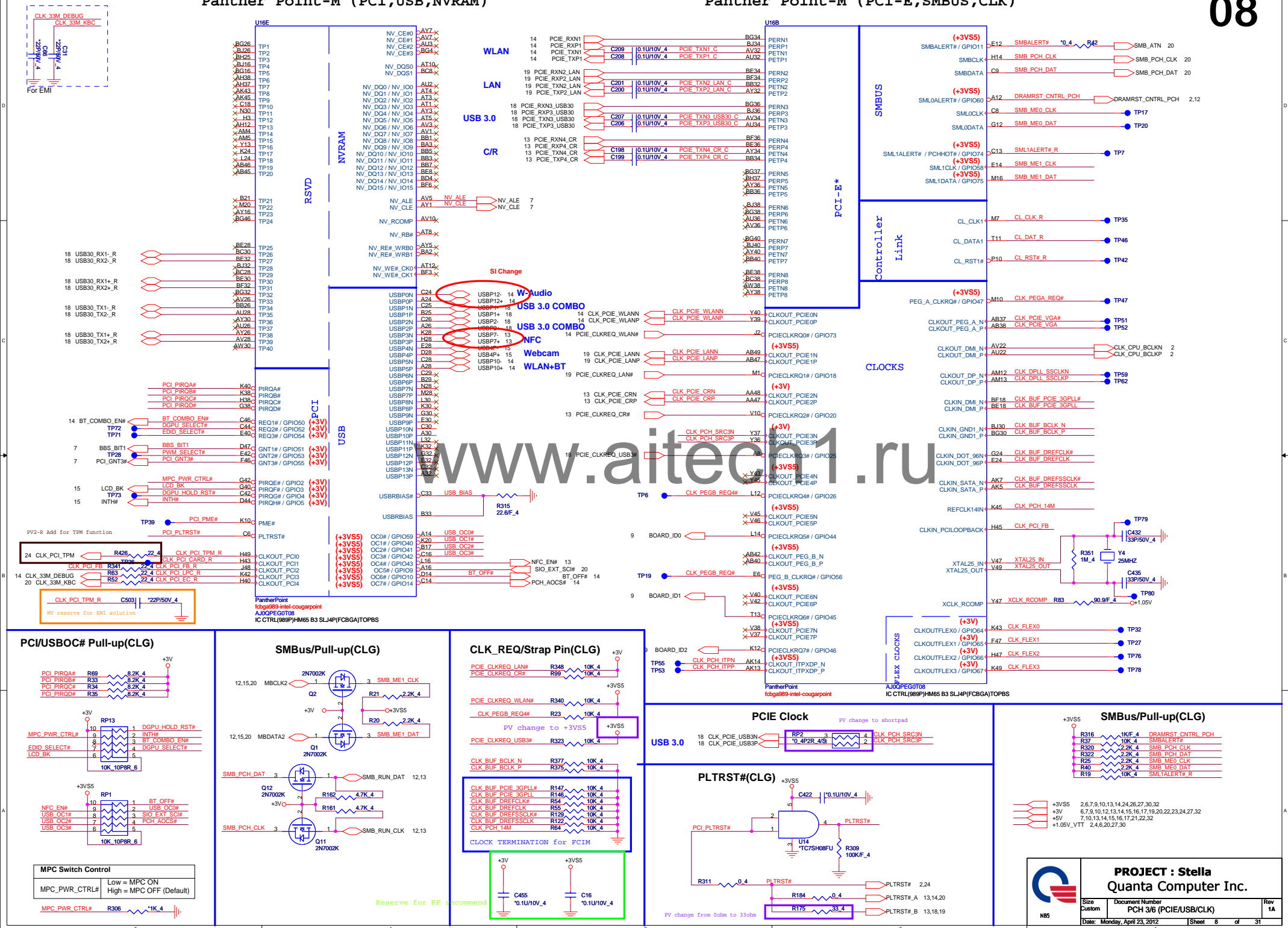


PROJECT : Stella
Quanta Computer Inc.

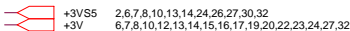
Size Custom	Document Number PCH 2/6 (SATA/HDA/SPI)	Rev 1A
Date: Monday, April 23, 2012	Sheet 7 of 31	

PCH Strap Table

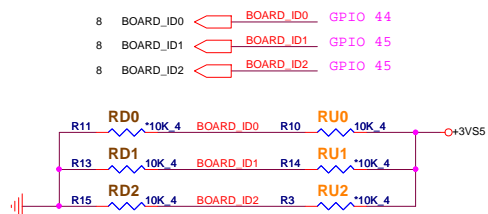
Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr><tr><td>1</td><td>0</td><td>SPI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	GNT1#	GNT0#	Boot Location	1	0	SPI	0	0	LPC	
GNT1#	GNT0#	Boot Location											
1	0	SPI											
0	0	LPC											
GPIO19	Different from Calpella Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)										
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28	Different from Calpella On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										



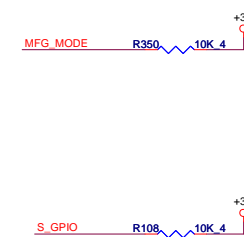
PV change to shortpad



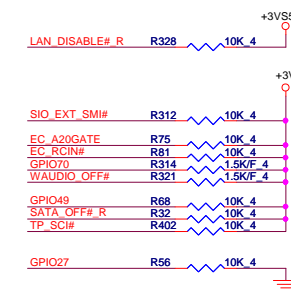
BOARD ID SETTING	BOARD_ID0 GPIO 44	BOARD_ID1 GPIO 45	BOARD_ID2 GPIO 46
HR	0	0	0
CR	1	0	0



MFG-TEST




GPIO Pull-up/Pull-down(CLG)



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Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable



BIOS RECOVERY	High = Disable (Default)
	Low = Enable

SV_SET_UP
High = Strong (Default)

TEST_DETECT
Low = Default

NATION
OVERRIDE

Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI TERMINATION
VOLTAGE OVERRIDE

LOW - Tx, Rx terminated to same voltage

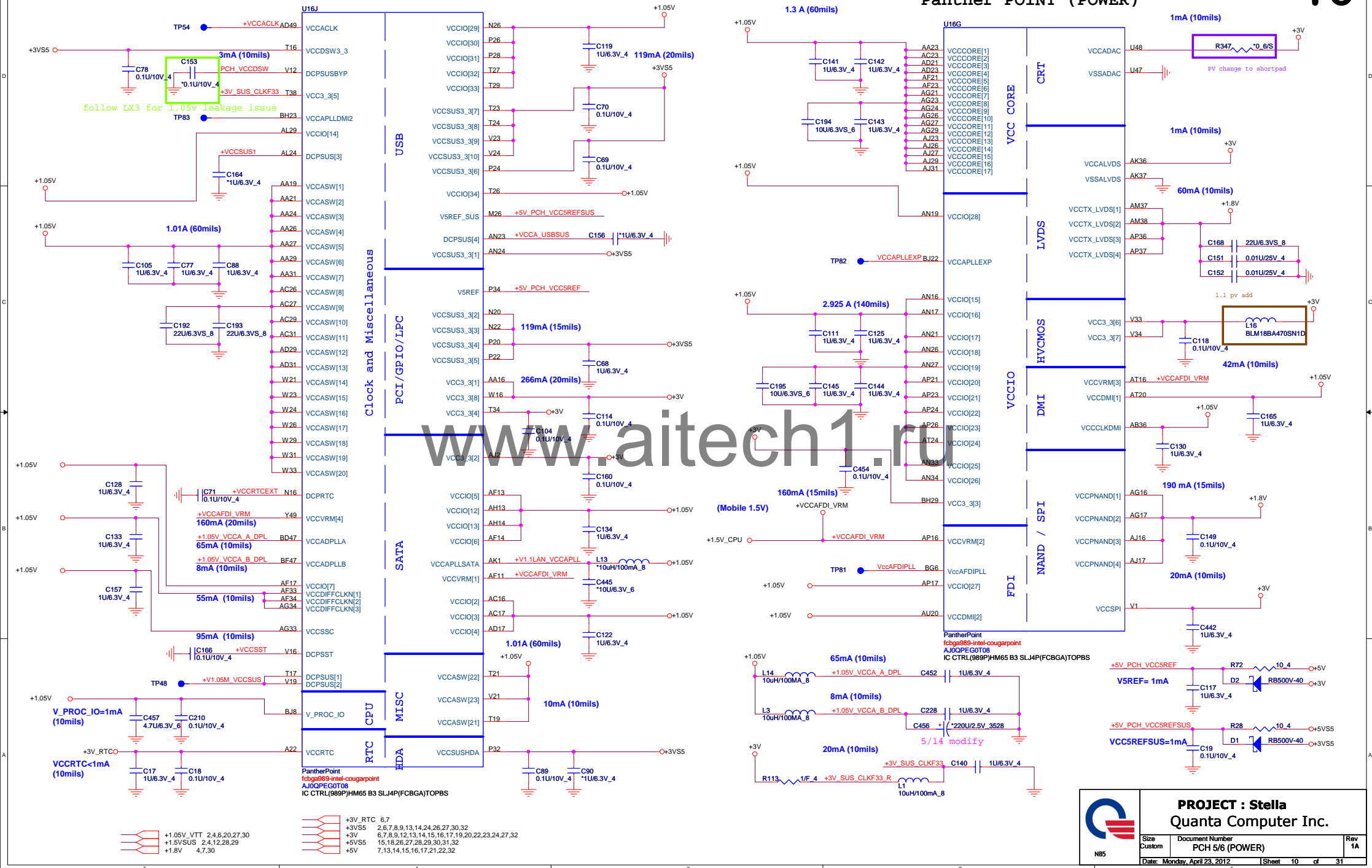


PROJECT : Stella
Quanta Computer Inc.

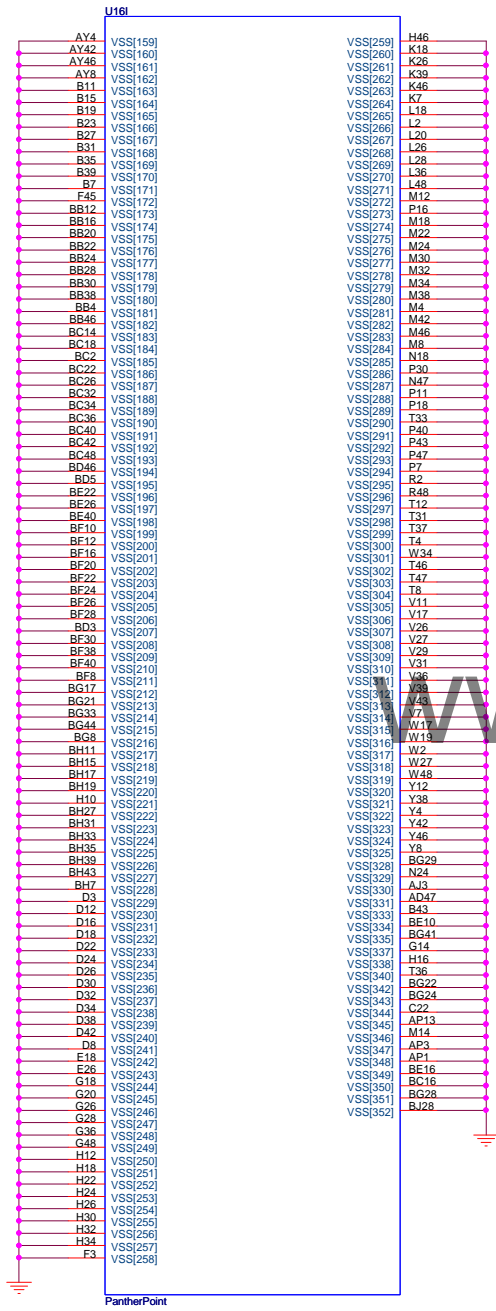
Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 1A
Date: Monday, April 23, 2012		Sheet 9 of 31

Panther Point (POWER)

Panther POINT (POWER)

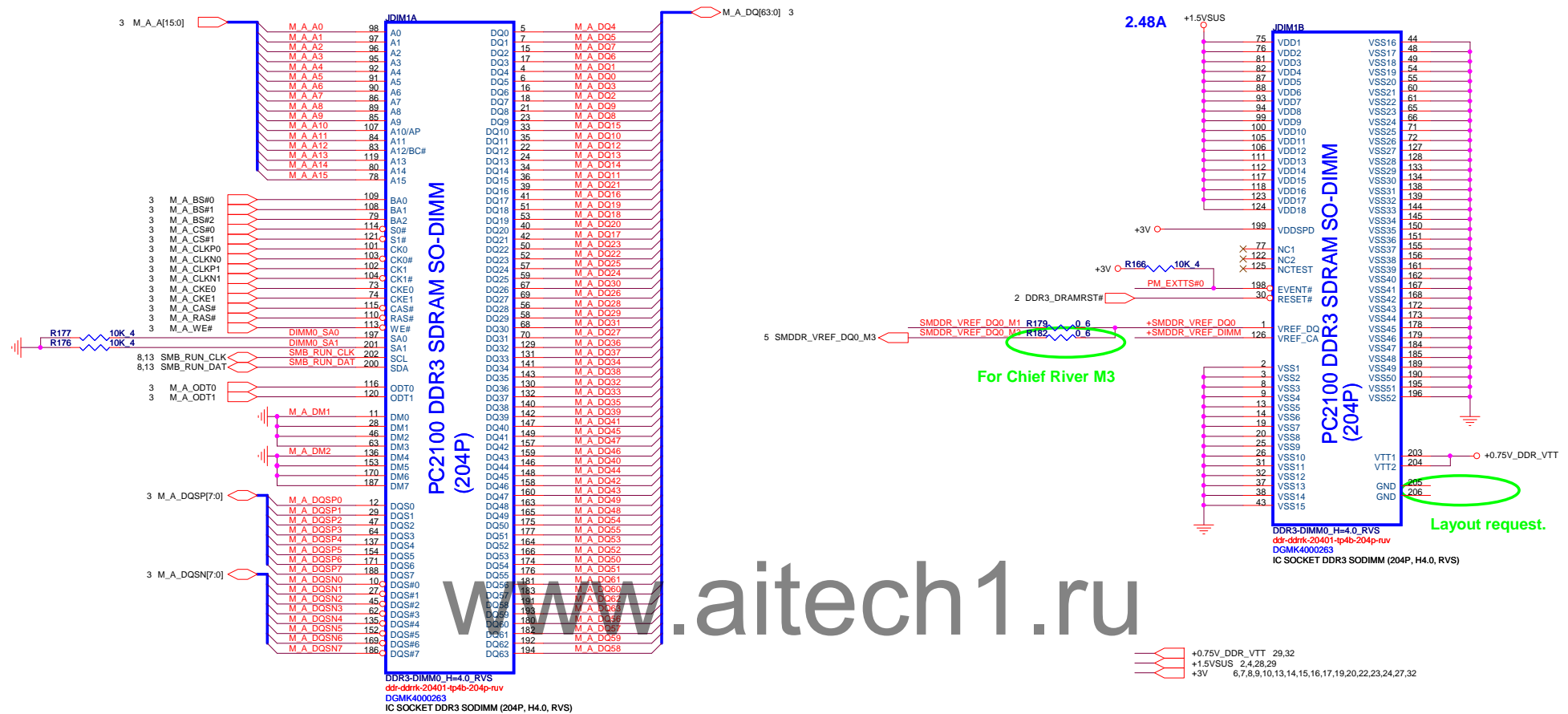


PantherPoint (GND)



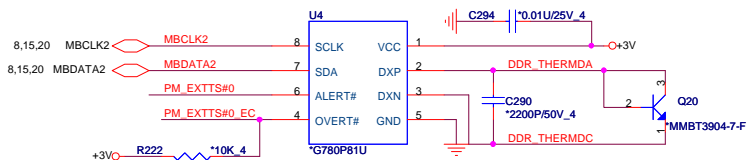
PantherPoint (GND)



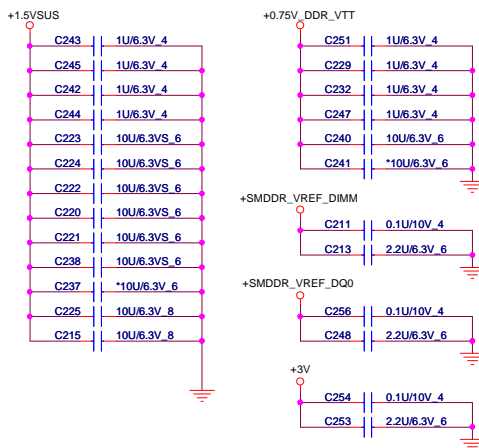


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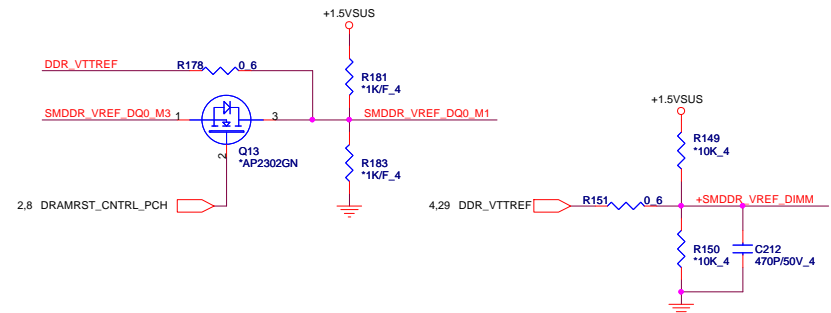
DDR3 Thermal Sensor



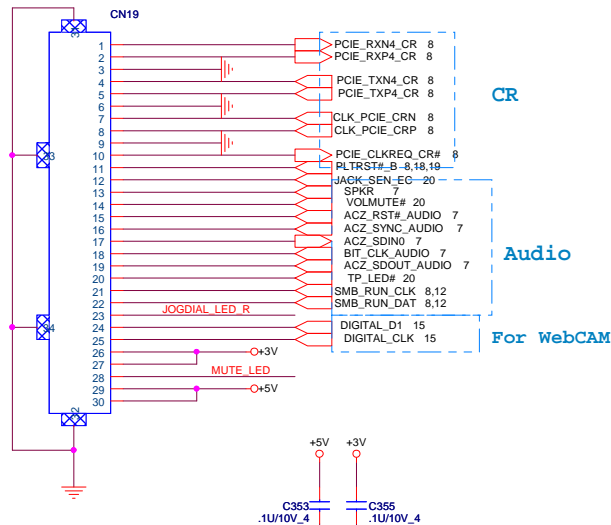
Place these Caps near So-Dimm0.



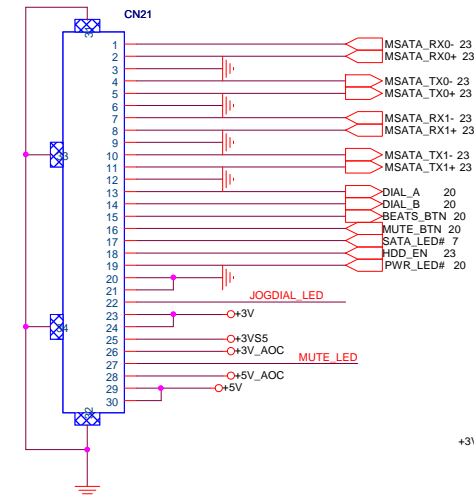
VREF DQ0 M1 Solution



FOR AUDIO/CR



FOR mSATA

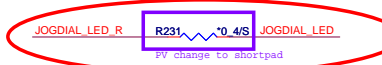
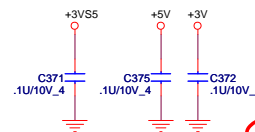


mSATA 1ST

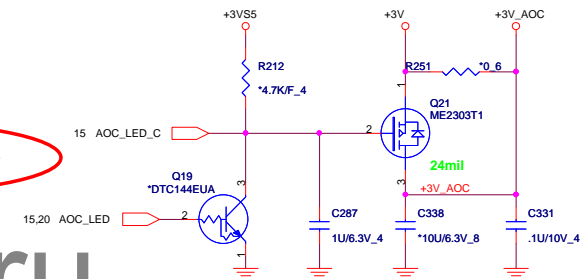
mSATA 2ND

JogDial

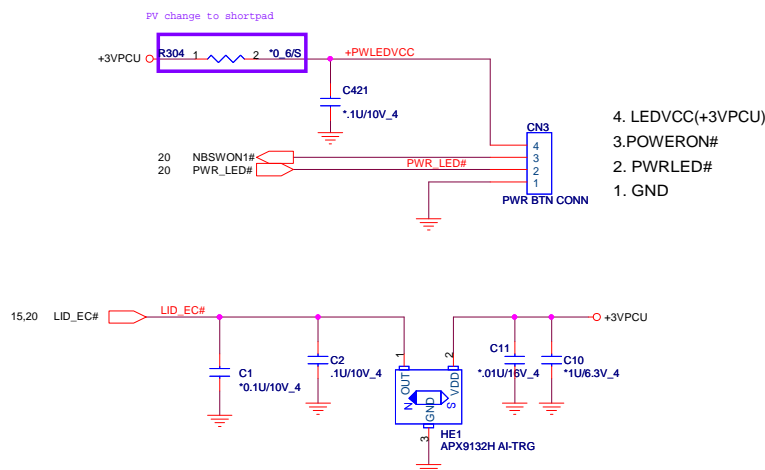
Mute Button



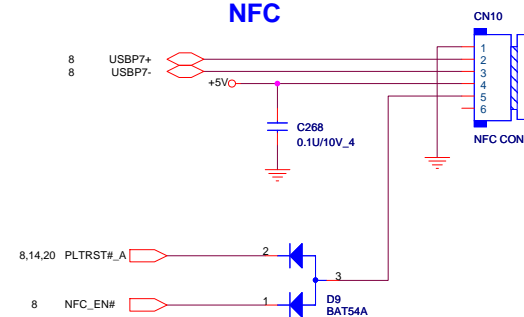
SI add



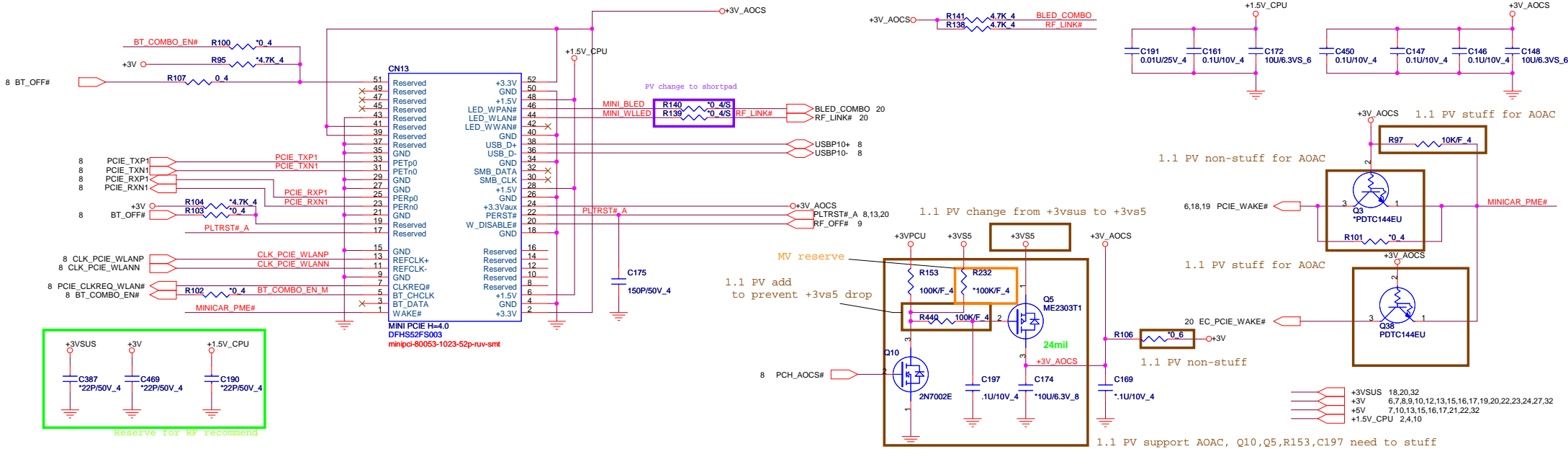
POWER BUTTON



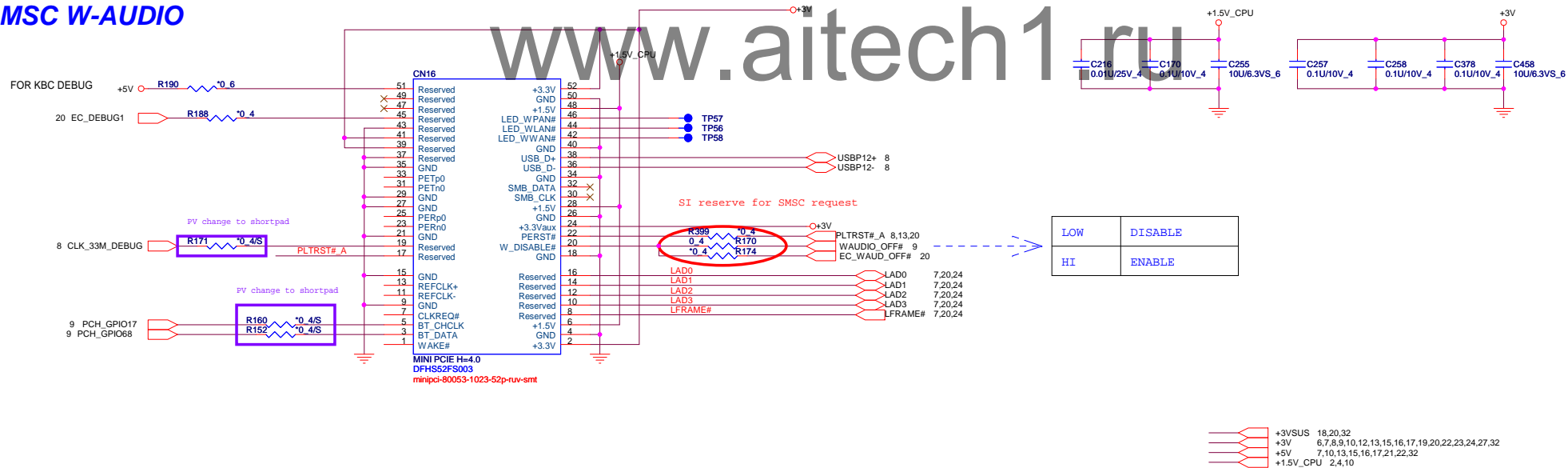
NFC

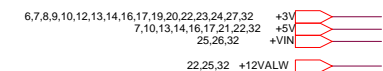
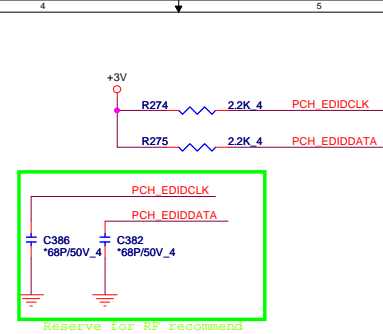


Mini PCI-E Card 1 WLAN+BT

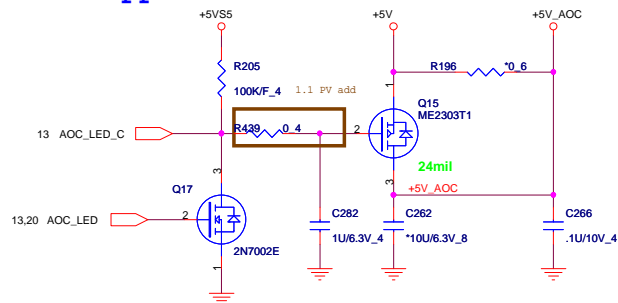


Mini PCI-E Card 1 SMSC W-AUDIO

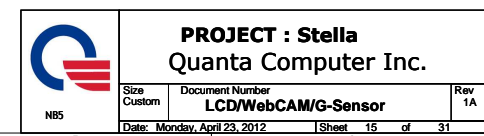
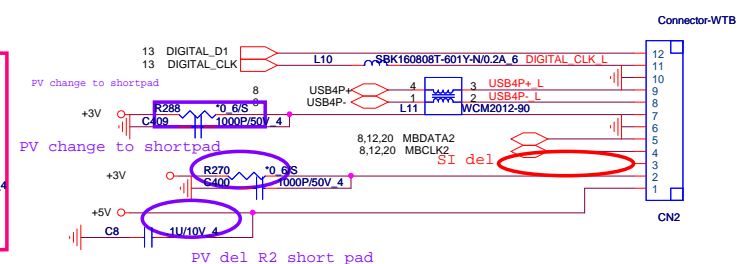
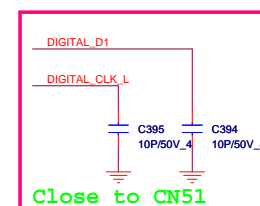
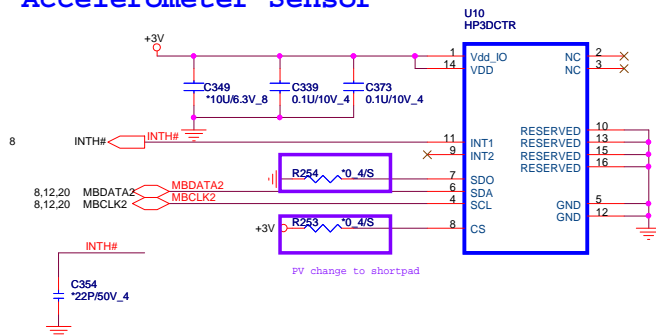




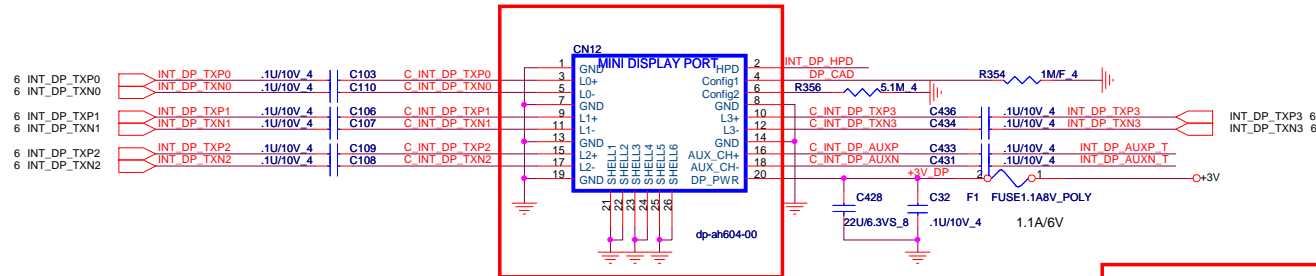
Support AOC function



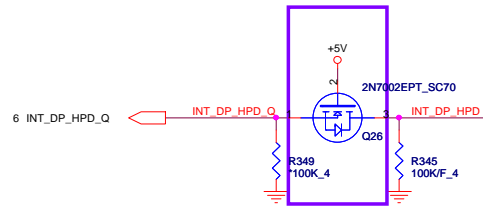
Accelerometer Sensor



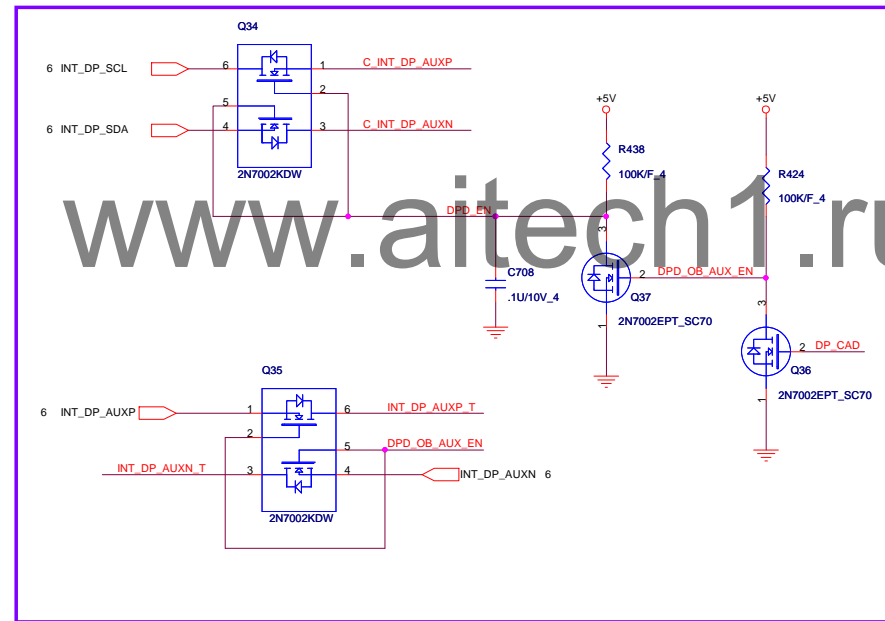
Mini Display



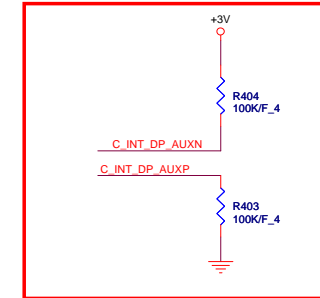
SI change footprint



PV change footprint to SC70

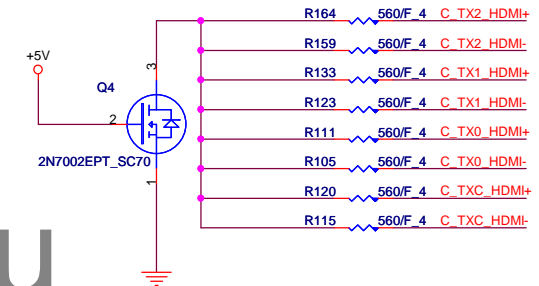
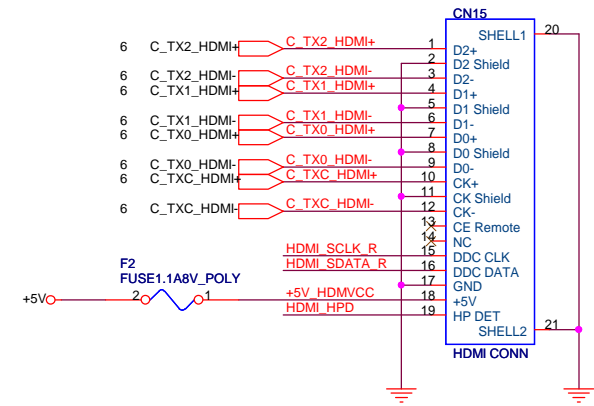
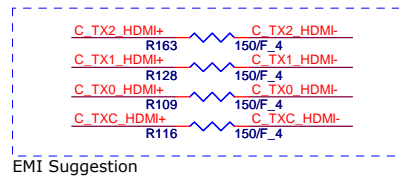
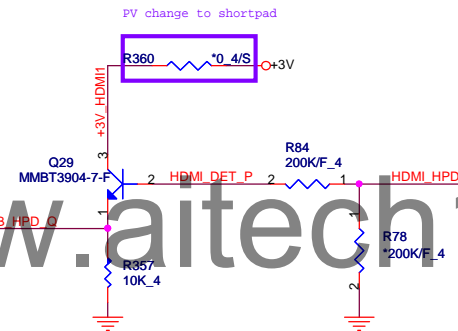
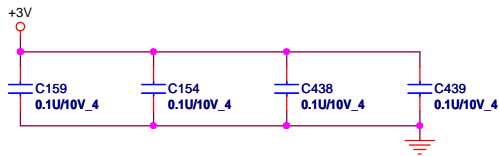
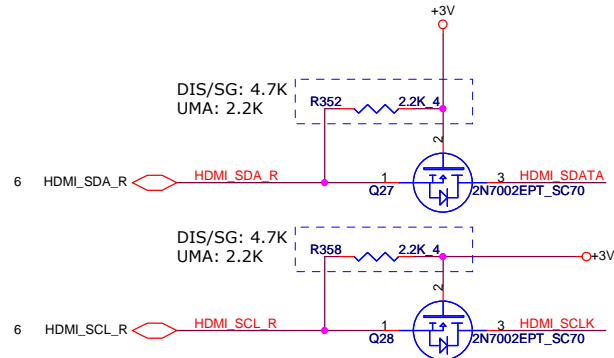
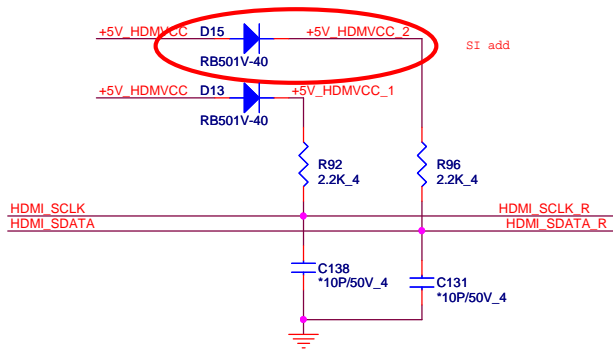


PV add for mini-display to HDMI dongle support



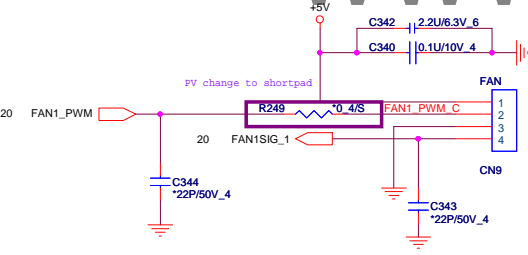
SI add for intel recommend

HDMI CON_COM

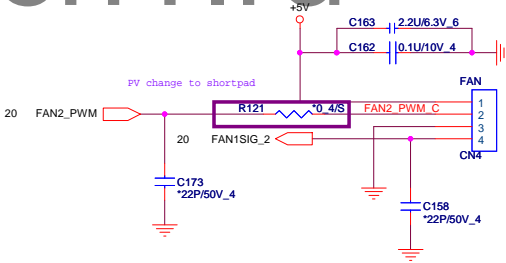


7,10,13,14,15,16,21,22,32 +5V
6,7,8,9,10,12,13,14,15,16,19,20,22,23,24,27,32 +3V

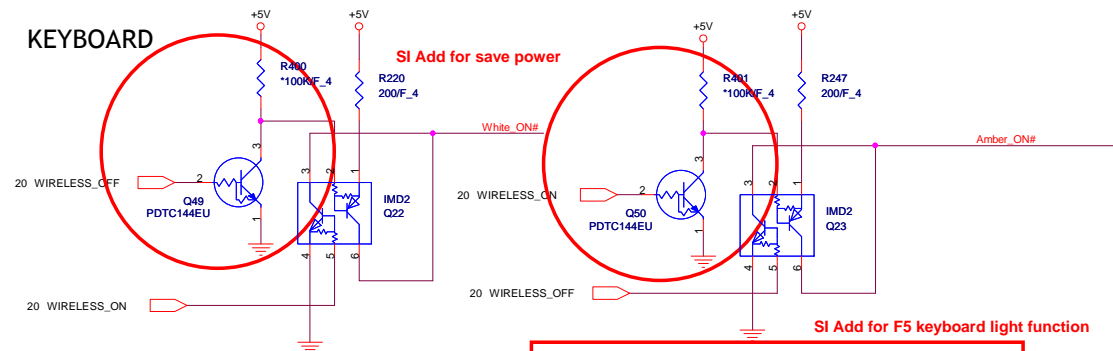
CPU FAN1



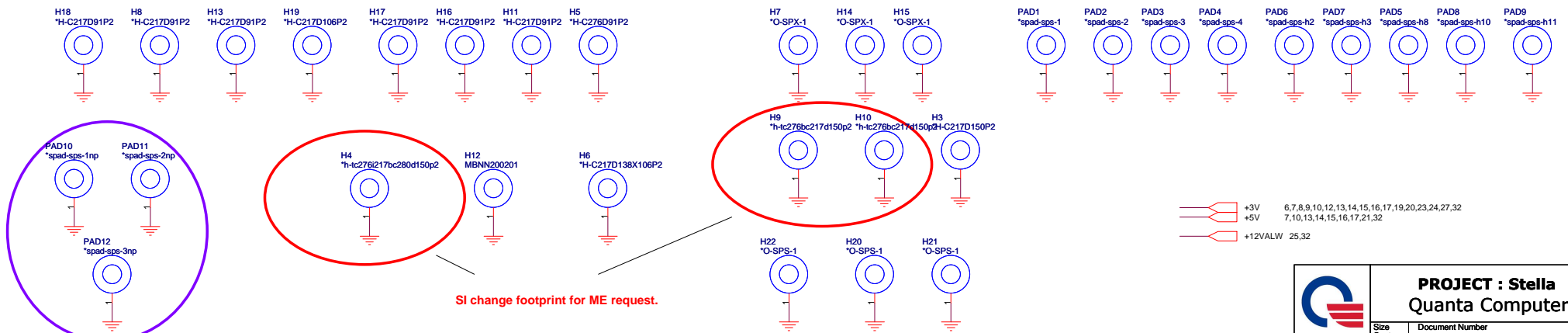
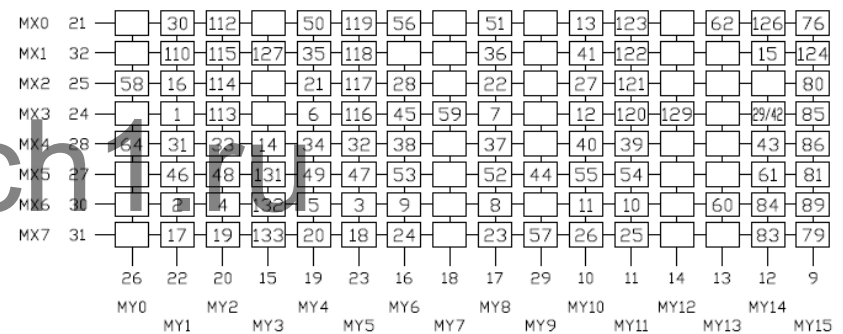
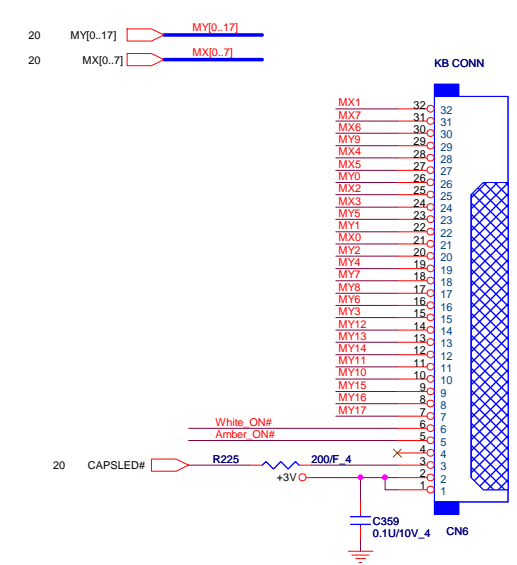
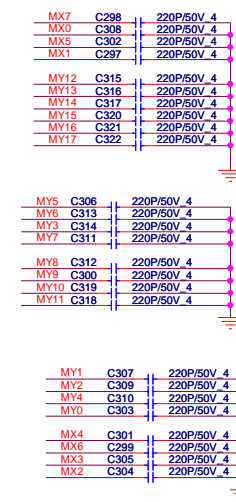
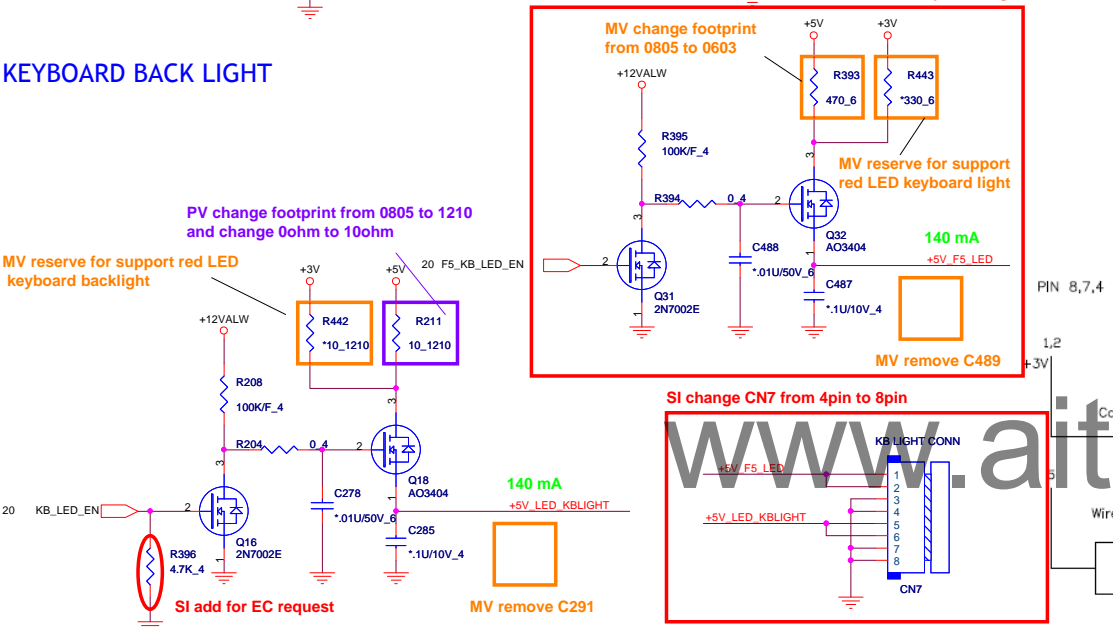
CPU FAN2



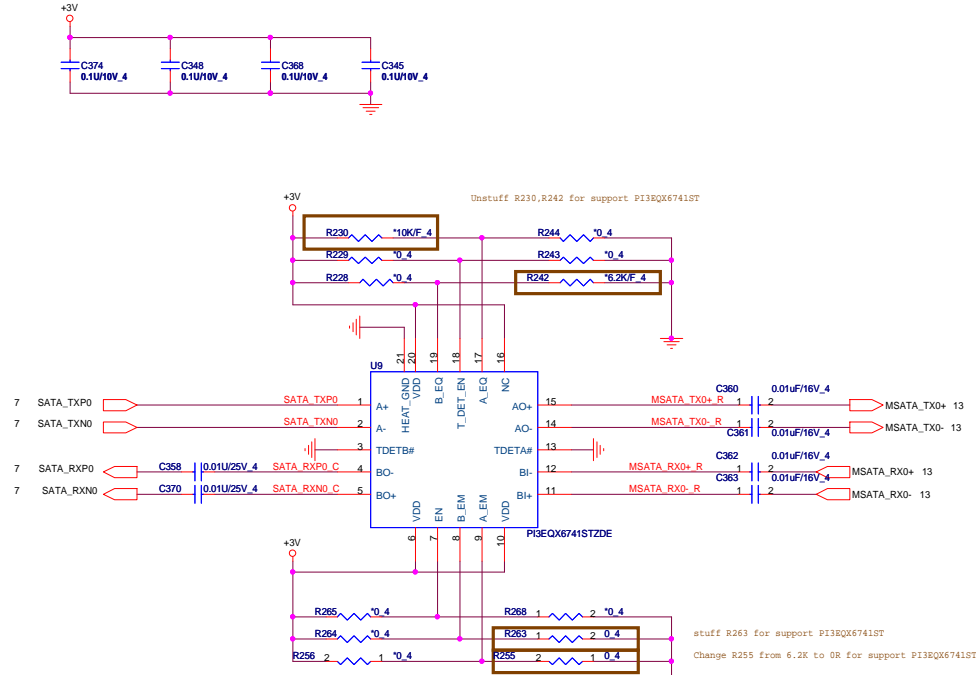
KEYBOARD



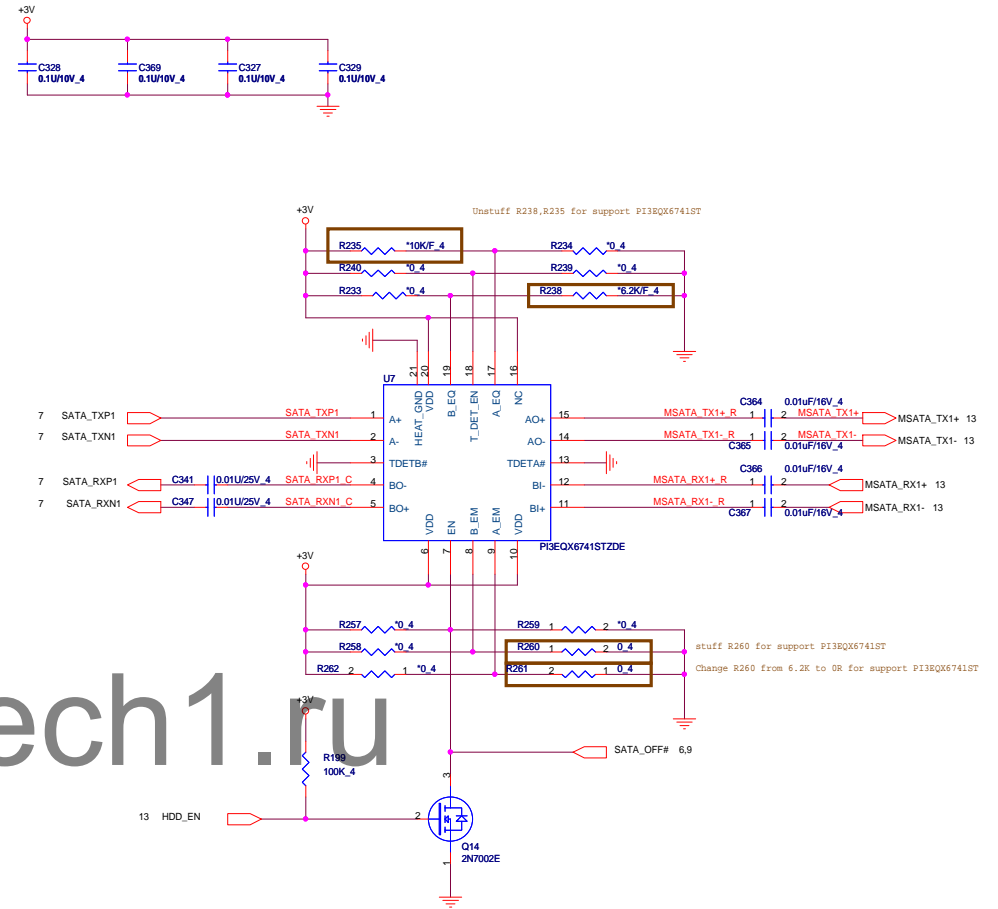
KEYBOARD BACK LIGHT



HDD0 mSATA 1ST



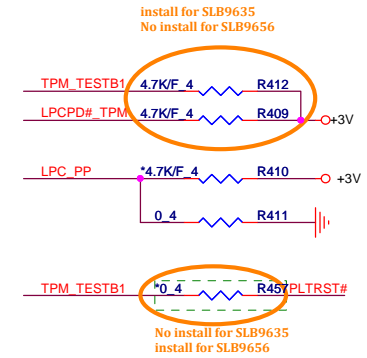
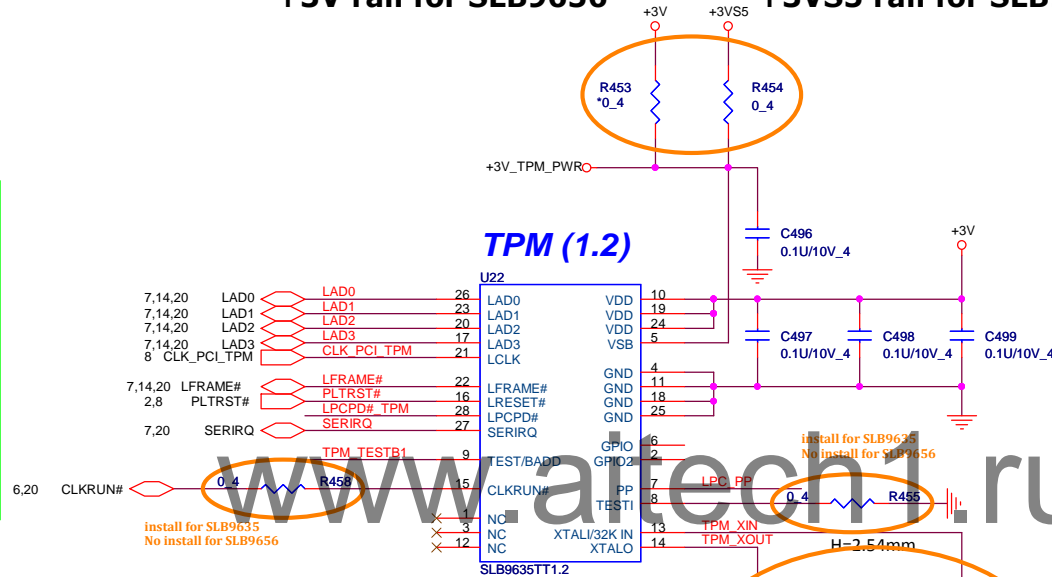
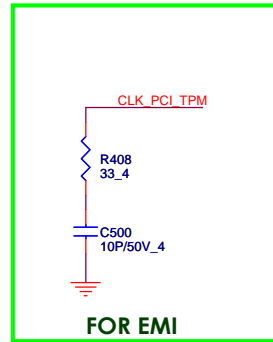
HDD1 mSATA 2ND



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+3V rail for SLB9656

+3VS5 rail for SLB9635



Address

	BADD
HIGH	4EH/4F

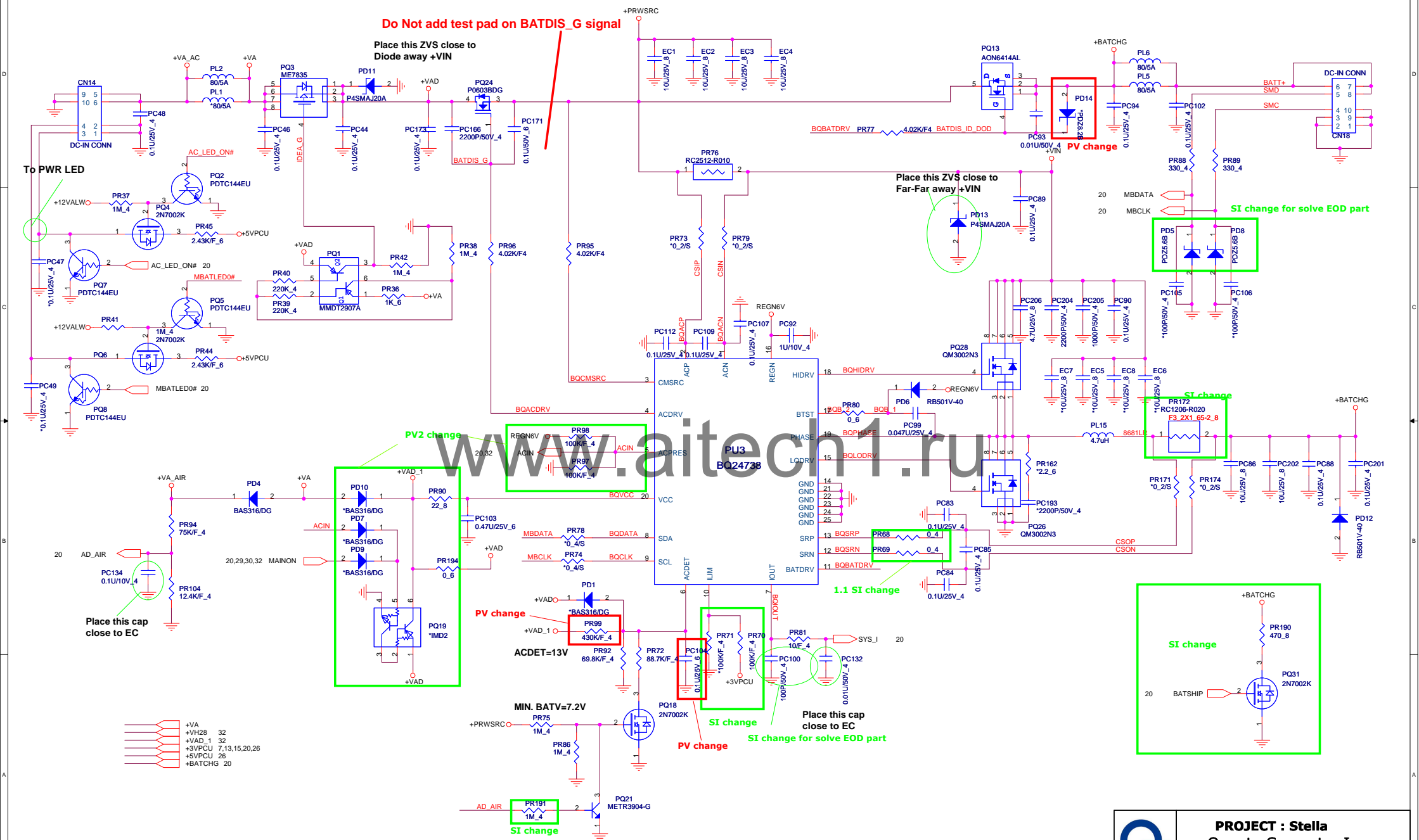
(default)

	SLB9635	SLB9656
R458	Install	No install
R453	No install	Install
R454	Install	No install
R455	Install	No install
Y6, R413	Install	No install
C501, C502	Install	No install
R412	Install	No install
R409	Install	No install
R457	No install	Install

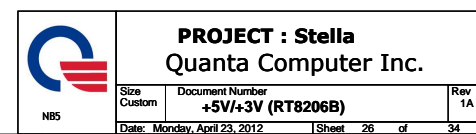
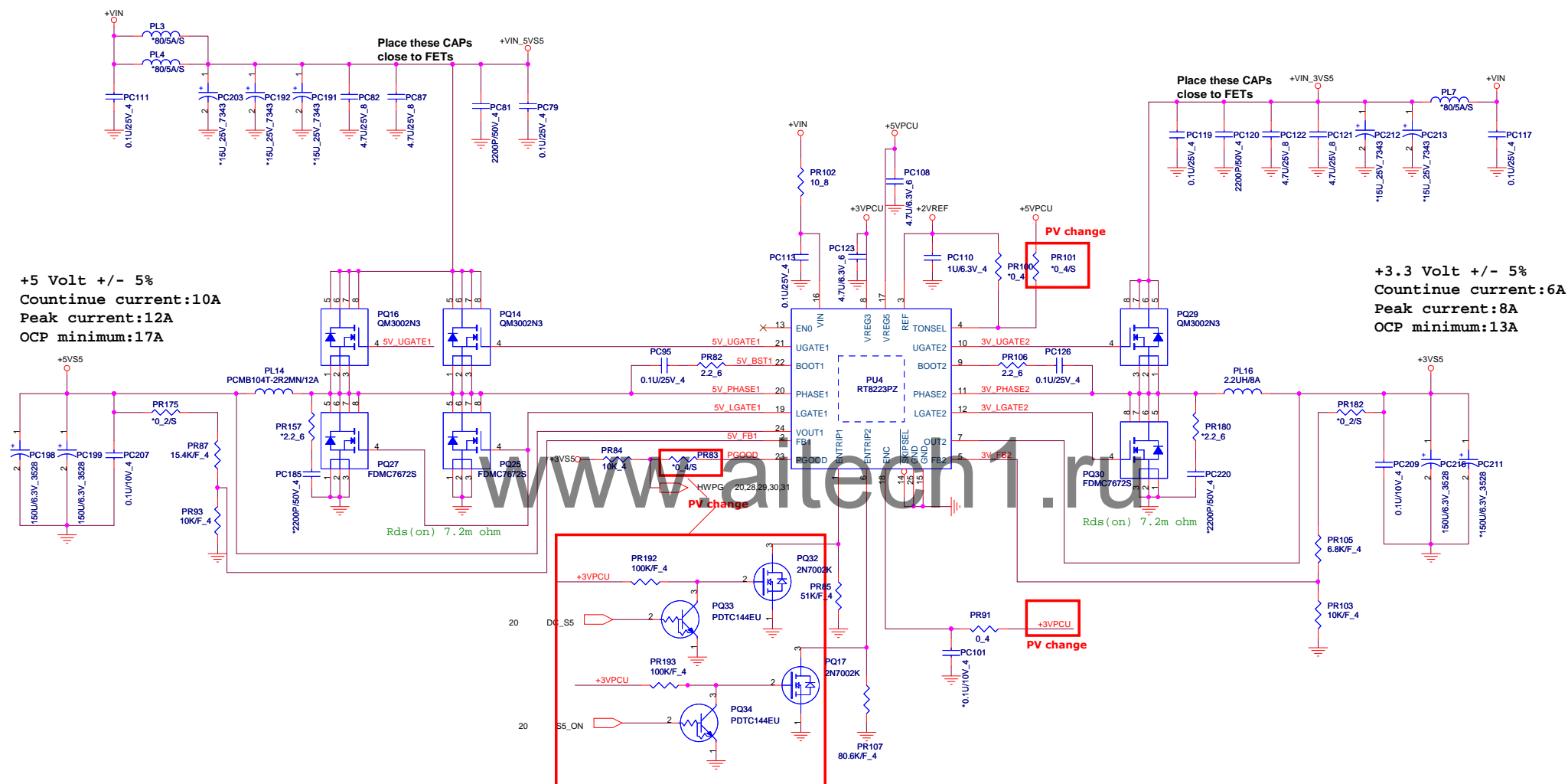


PROJECT : SPS
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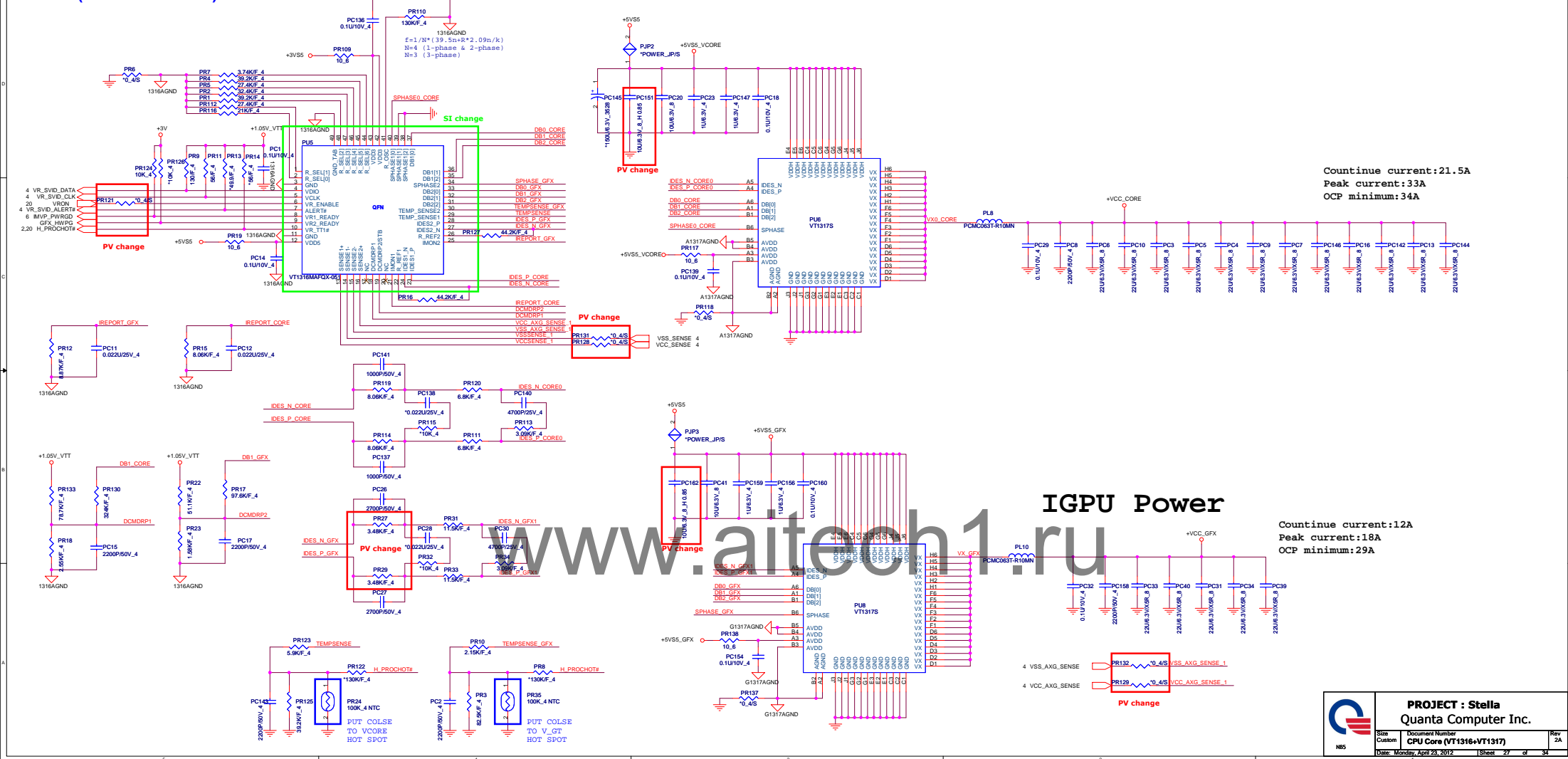
Size	Document Number	Rev
B	TPM	1A
Date: Monday, April 23, 2012	Sheet 24 of 34	



DC/DC +3VS5/+5VS5



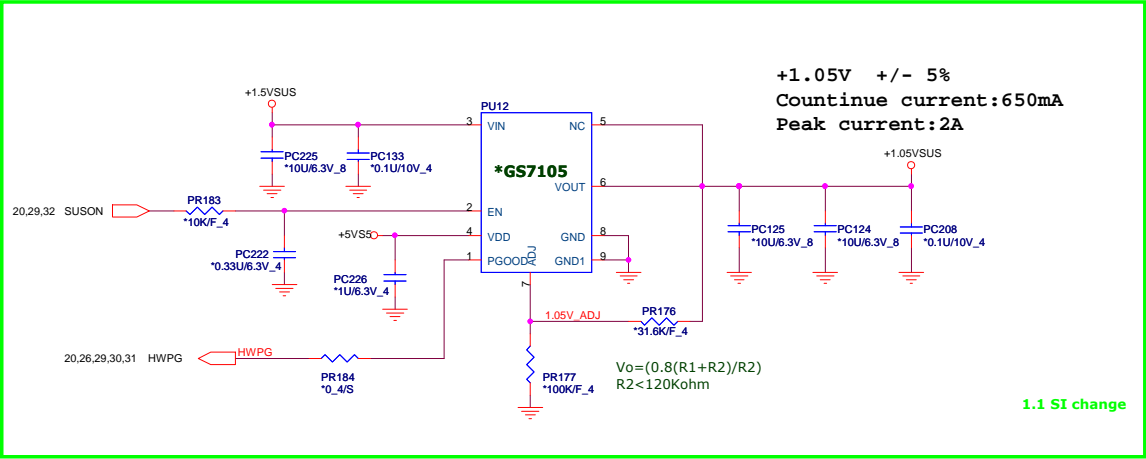
CPU Core(VT1316M+VT317S)

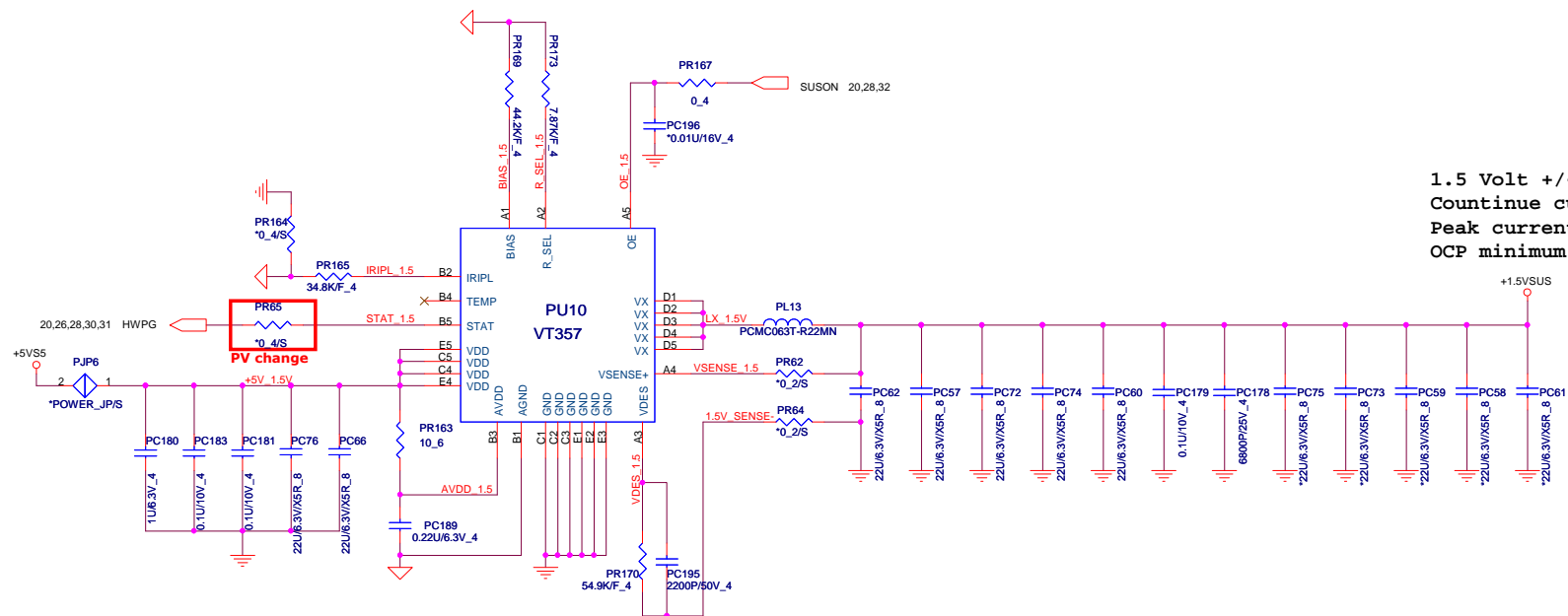


VCCP1.05V

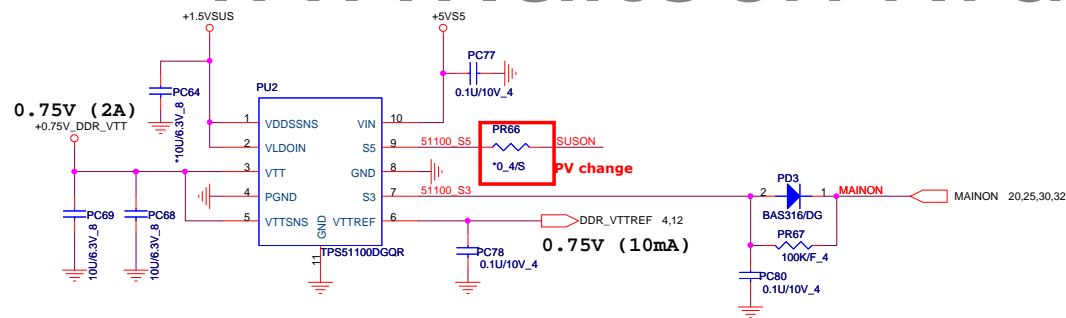
PV Deleted

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CPU system agent
voltage slew rate of 0.5 -10 mV/μs

H_FC_C22 VID0	VCCSA_SEL VID1	Vout
0	0	0.9V
0	1	0.85V
1	0	0.725V
1	1	0.675V

